

nanoSoC Datasheet

SoC Labs

November 20, 2024

Preamble, copyrights licenses etc.

Contents

1	Introduction	3
1.1	Summary	3
2	System	4
2.1	Bus Interconnect	4
2.2	Address Map	4
2.2.1	Summary	4
2.2.2	System IO Region	4
2.3	5
3	Peripherals	6
4	Recommended Testboard	7

Chapter 1

Introduction

1.1 Summary

Chapter 2

System

2.1 Bus Interconnect

2.2 Address Map

2.2.1 Summary

Region	Start Address	End Address
Boot-Rom	0x00000000	0x0FFFFFFF
Instruction Memory (SRAM)	0x20000000	0x2FFFFFFF
Data Memory (SRAM)	0x30000000	0x3FFFFFFF
System IO	0x40000000	0x5FFFFFFF
Expansion IO	0x60000000	0x7FFFFFFF
Expansion Memory Lo (SRAM)	0x80000000	0x8FFFFFFF
Expansion Memory Hi (SRAM)	0x90000000	0x9FFFFFFF
Expansion IO	0xA0000000	0xDFFFFFFF
System Table ROM	0xF0000000	0xF0003FFF

2.2.2 System IO Region

Below are the address regions for the System IO/Peripherals, detailed address maps for each peripheral are in chapter 3

Region	Start Address	End Address
Timer 0	0x40000000	0x40000FFF
Timer 1	0x40001000	0x40001FFF
Dual Timer	0x40002000	0x40003FFF
UART 0	0x40004000	0x40004FFF
UART 1	0x40005000	0x40005FFF
UART 2	0x40006000	0x40007FFF
Watchdog Timer	0x40008000	0x40008FFF
USRT 2	0x4000E000	0x4000EFFF
DMA 0 Base	0x4000F000	0x4000EFFF
GPIO 0	0x40010000	0x40010FFF
GPIO 1	0x40011000	0x40011FFF
System Control	0x4001F000	0x4001FFFF

2.3

Chapter 3

Peripherals

Chapter 4

Recommended Testboard